

FIG. 1

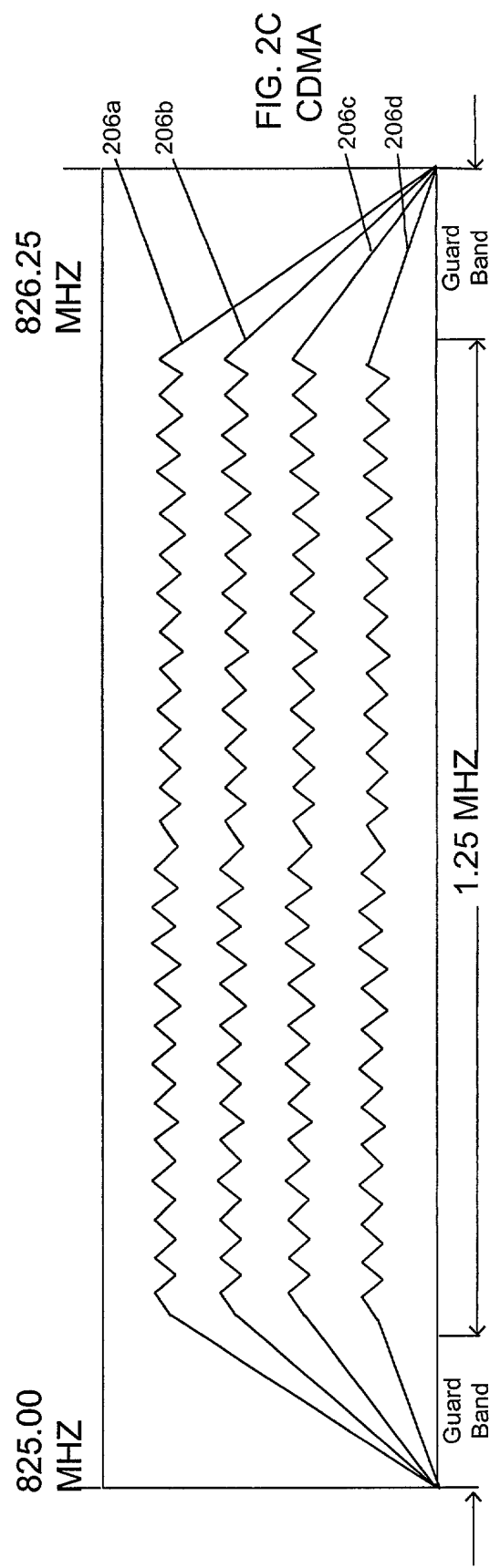
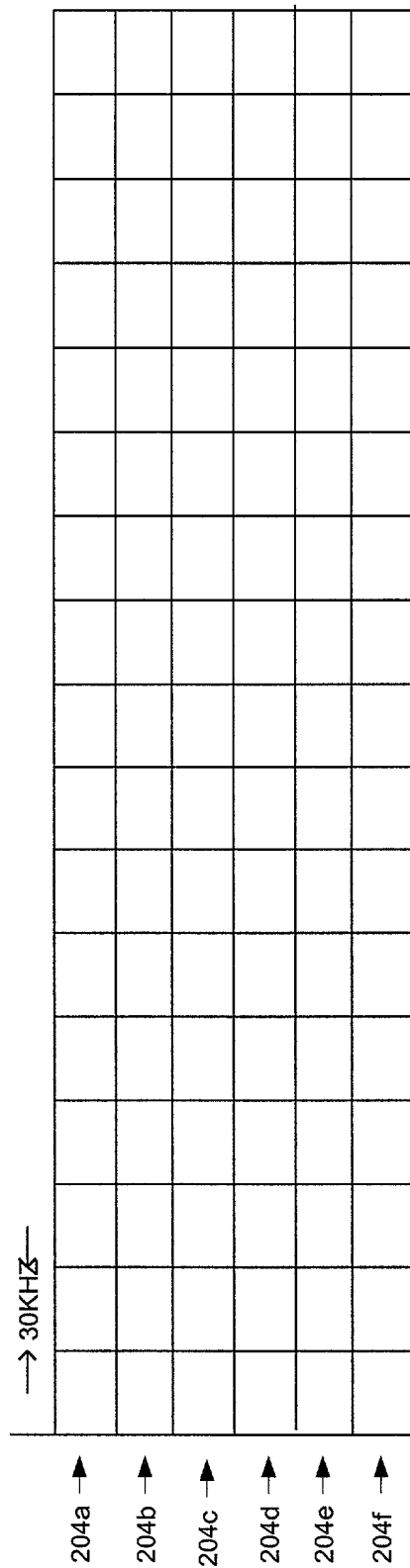
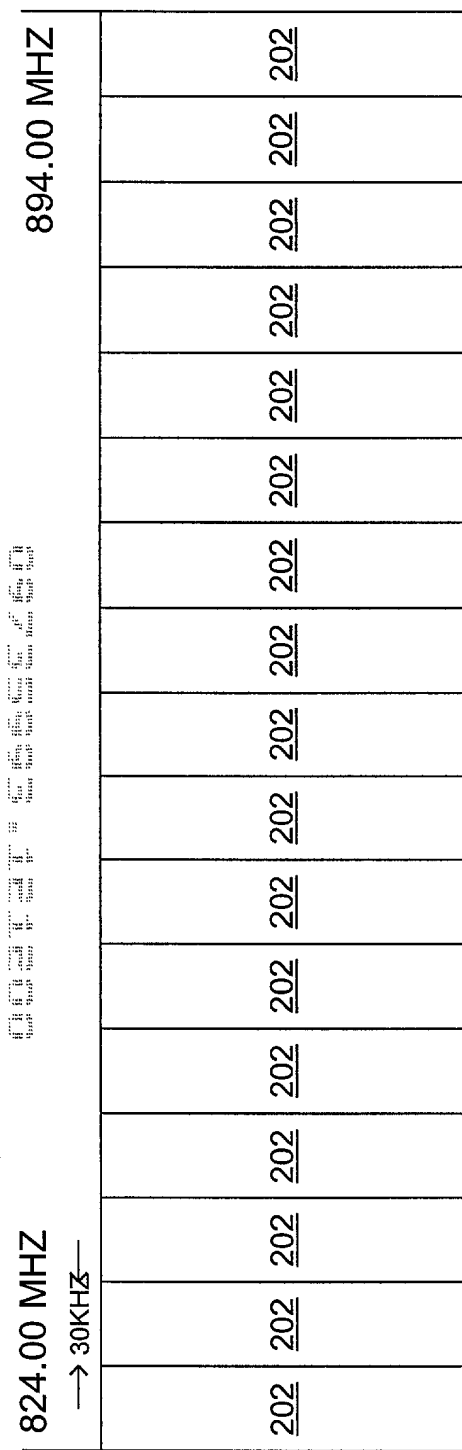


FIG. 3A is a block diagram of a transmitter 300. The transmitter 300 includes a baseband processor 302, two DACs 304 and 306, a multiplier 308, two multipliers 310 and 312, a power amplifier 316, and an antenna 318. The baseband processor 302 outputs I and Q signals to the DACs 304 and 306. The DAC 304 outputs a signal to the multiplier 308. The DAC 306 outputs a signal to the multiplier 310. The multiplier 308 outputs a signal to the multiplier 312. The multiplier 312 outputs a signal to the power amplifier 316. The power amplifier 316 outputs a signal to the antenna 318.

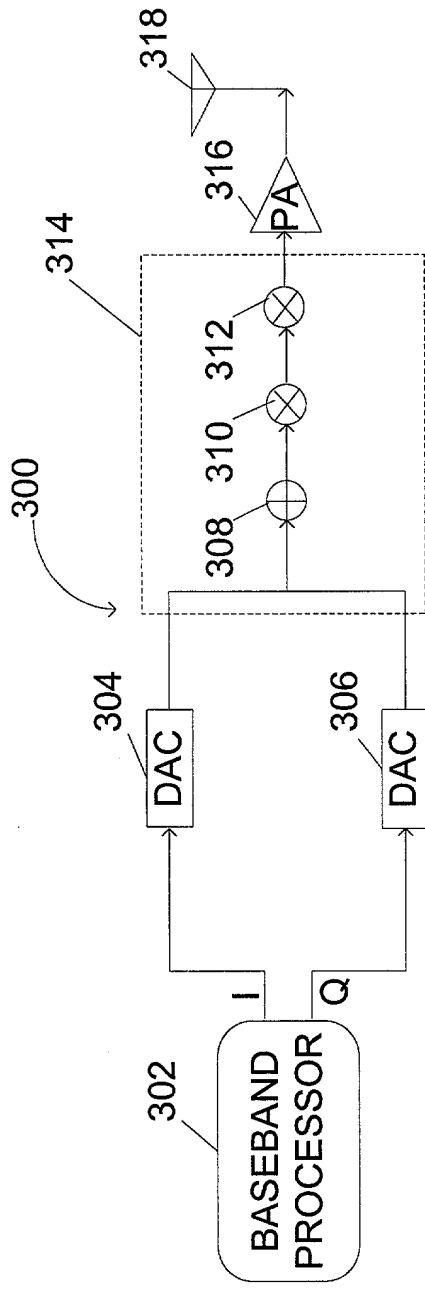


FIG. 3A

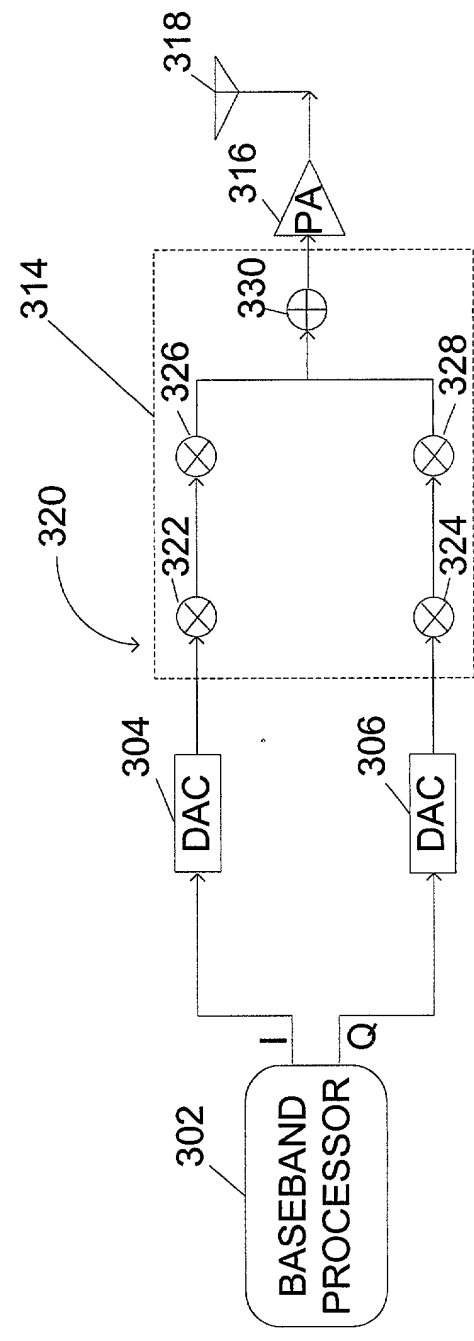


FIG. 3B

FIG. 4 is a diagram illustrating a mapping of Symbol States to I and Q components and Symbol Bit Patterns.

Symbol State	I	Q	Symbol Bit Pattern	Phase State
1	1	1	00	45°
2	-1	1	10	135°
3	-1	-1	11	225°
4	1	-1	01	315°

FIG. 4

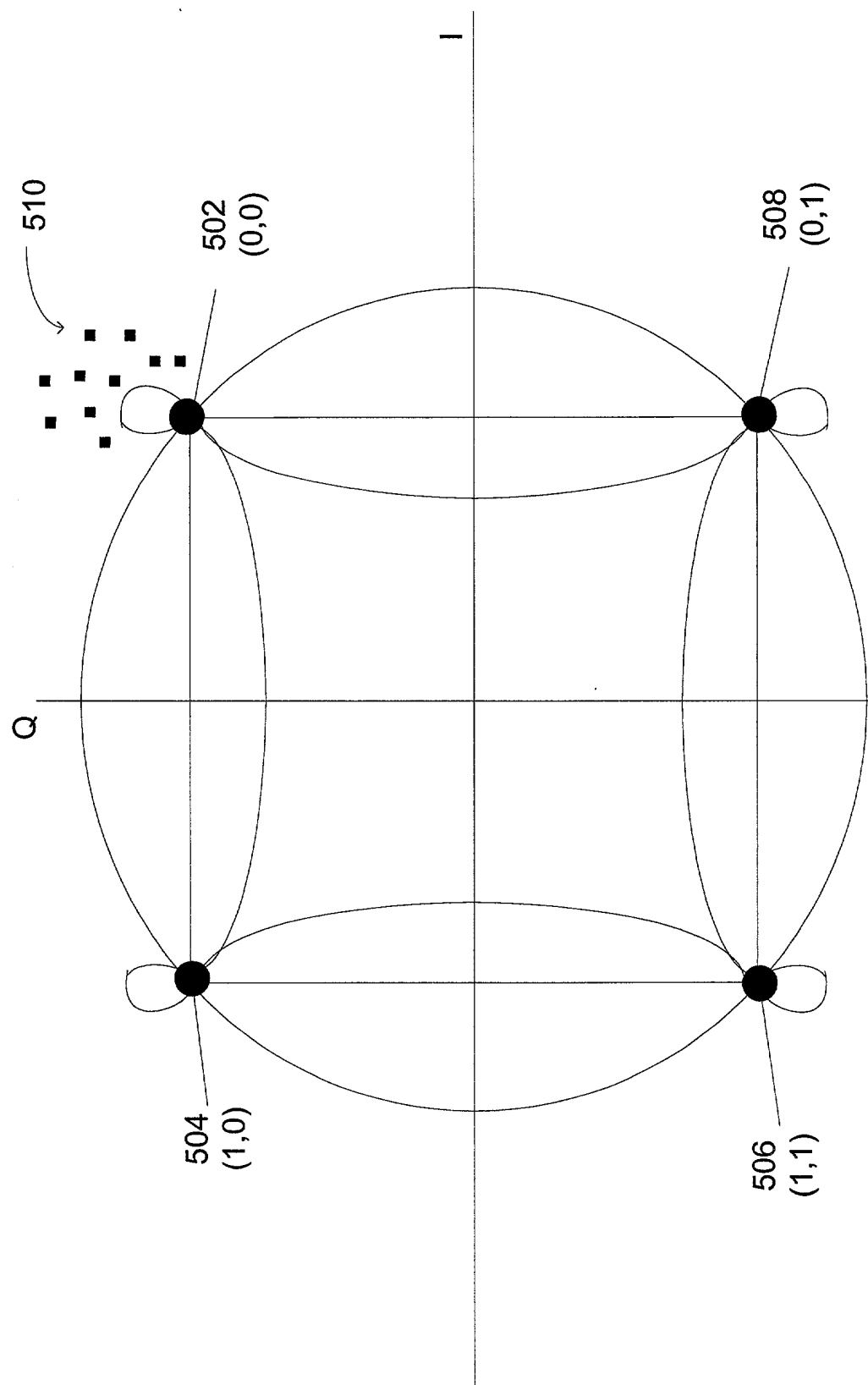


FIG. 5

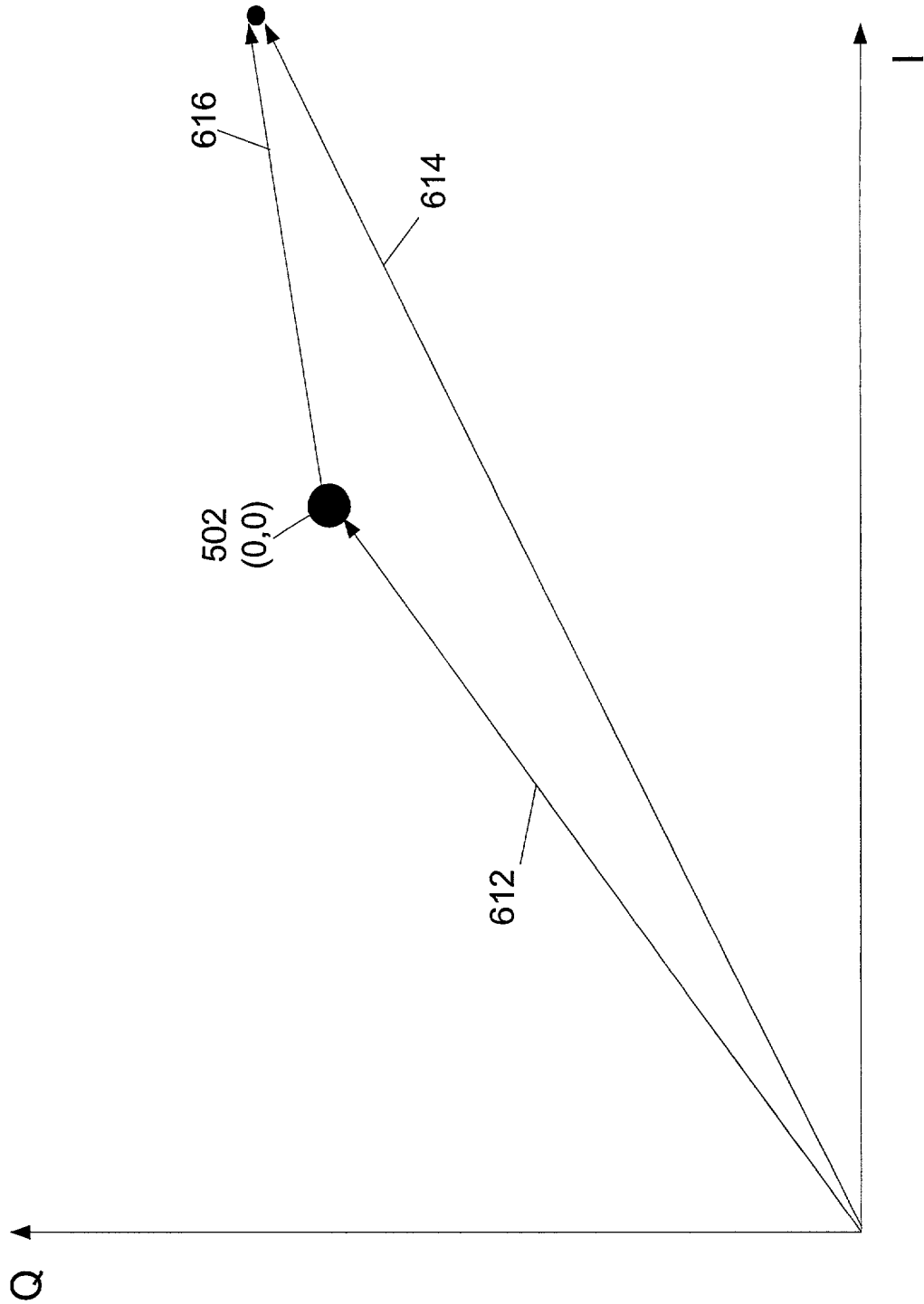


FIG. 6

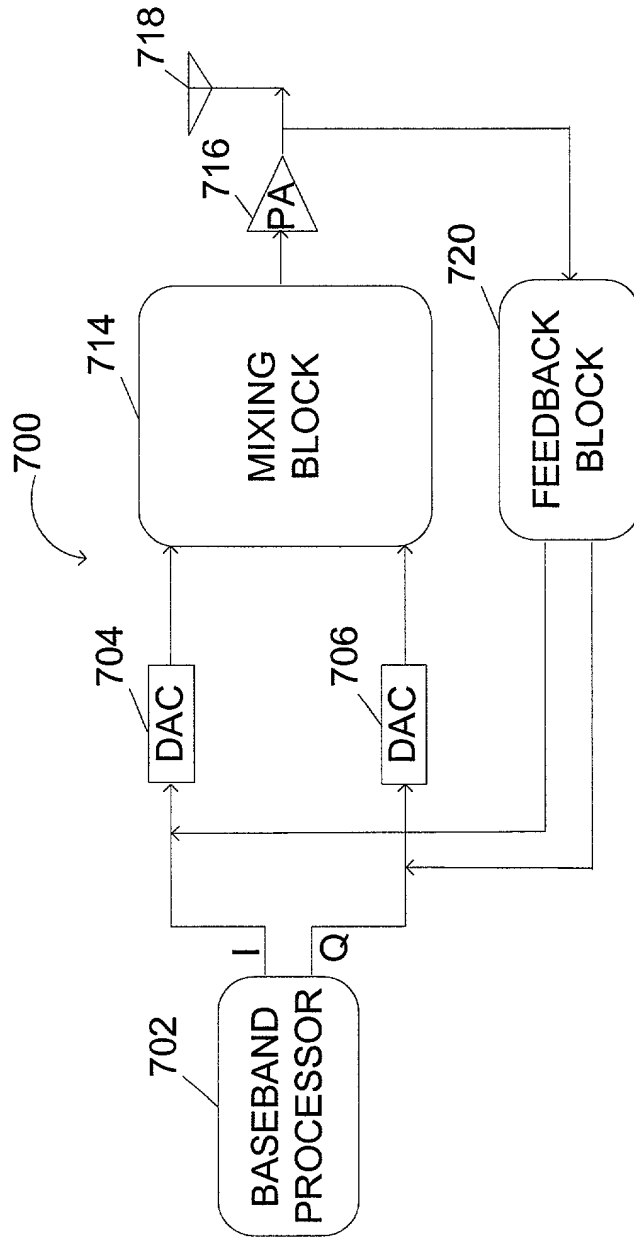


FIG. 7

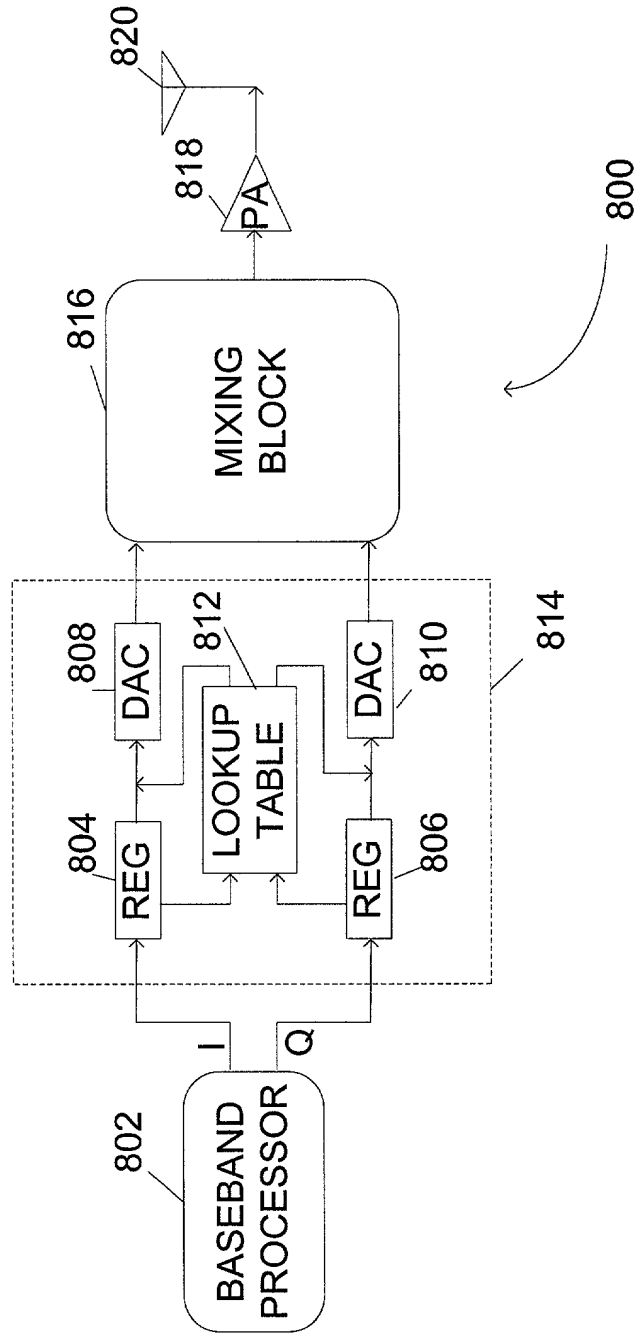


FIG. 8



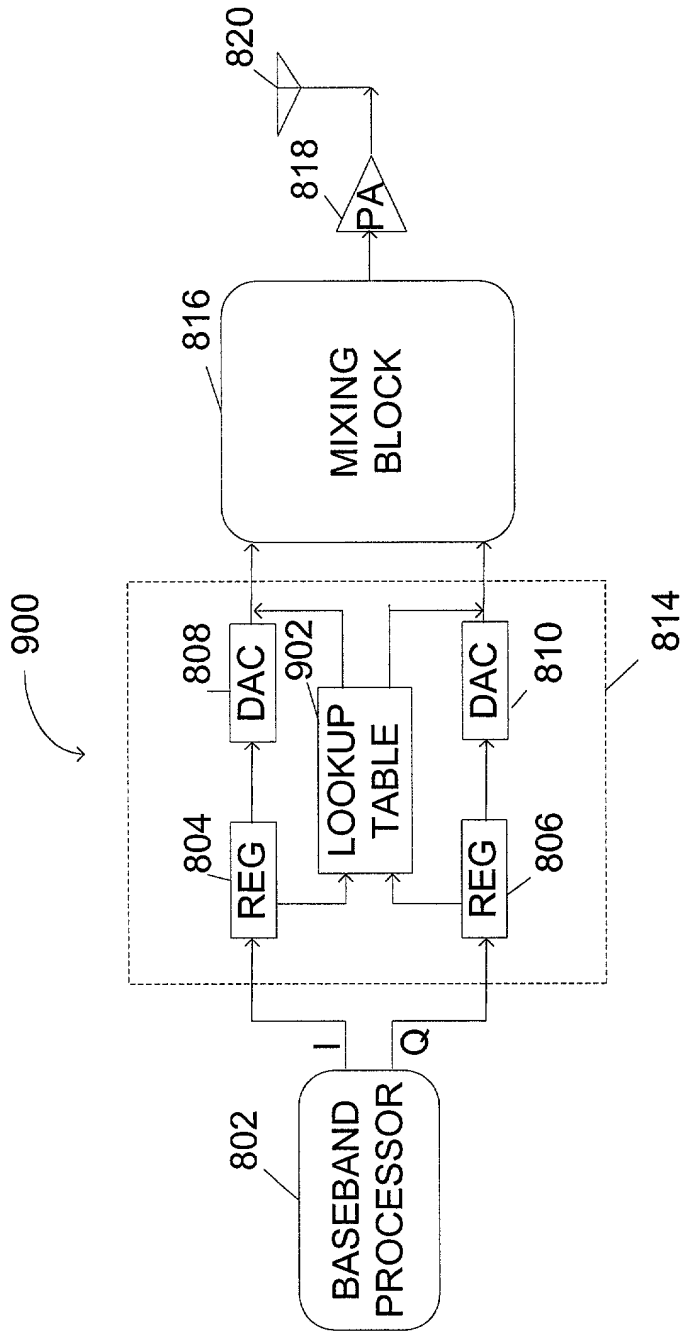


FIG. 9

1000

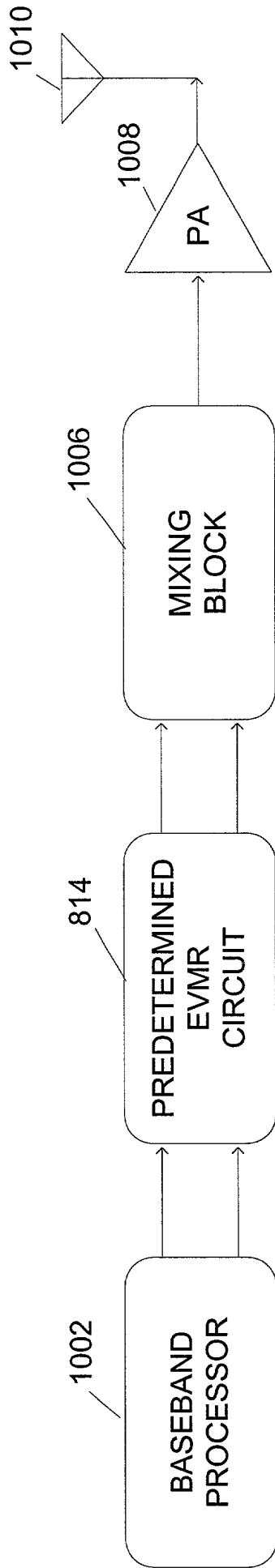


FIG. 10

FIG. 11 is a flowchart illustrating a process for determining a bit pattern.

FIG. 11

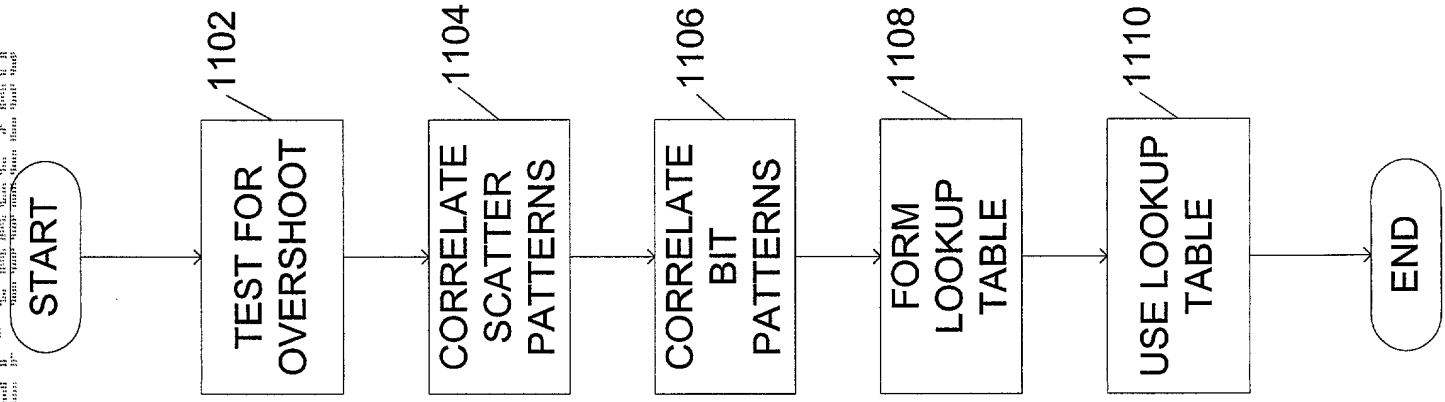


FIG. 12

